

Claims

- [c1] An electronic device comprising:
a semiconductor substrate having an array of gate conductors, each having a length and a width, comprised of dummy gate conductors and functional gate conductors extending in a widthwise direction, said gate conductors positioned substantially parallel to each other in said widthwise direction and periodically spaced apart a fixed distance in a direction substantially perpendicular to said widthwise direction.
- [c2] The electronic device of claim 1, wherein said functional gate conductors include conductors of at least two different widths.
- [c3] The electronic device of claim 1, wherein said dummy gate conductors include conductors of at least two different widths.
- [c4] The electronic device of claim 1, wherein said dummy gate conductors and functional gate conductors include conductors of the same width.
- [c5] The electronic device of claim 1, further comprising additional dummy gate conductors positioned adjacent to ends of said functional gate conductors.
- [c6] The electronic device of claim 5, wherein said additional dummy gate conductors are the same width as one of said functional gate conductors.

- [c7] The electronic device of claim 1, wherein the length of said functional gate conductors is a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance.
- [c8] The electronic device of claim 1, wherein the length of said dummy gate conductors is a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance.
- [c9] The electronic device of claim 1, further including source/drains formed in said substrate underneath and proximate to said functional gate conductors.
- [c10] The electronic device of claim 1, further including N-wells, P-wells or both N-wells and P-wells formed in said substrate underneath and proximate to said functional gate conductors.
- [c11] The electronic device of claim 1, further including a gate dielectric formed between said gate conductors and said substrate.
- [c12] A method of fabricating an electronic device comprising:
providing a semiconductor substrate; and
forming on said substrate, an array of gate conductors, each having a length and a width, comprised of dummy gate conductor and functional gate conductors extending in a widthwise direction, said gate conductors positioned

substantially parallel to each other in said widthwise direction and periodically spaced apart a fixed distance in a direction substantially perpendicular to said widthwise direction.

- [c13] The method of claim 12, wherein said functional gate conductors include conductors of at least two different widths.
- [c14] The method of claim 12, wherein said dummy gate conductors include conductors of at least two different widths.
- [c15] The method of claim 12, wherein said dummy gate conductors and functional gate conductors include conductors of the same width.
- [c16] The method of claim 12, further comprising forming additional dummy gate conductor positioned adjacent to ends of said functional gate conductors.
- [c17] The method of claim 16, wherein said additional dummy gate conductors are the same width as one of said functional gate conductors.
- [c18] The method of claim 12, wherein the length of said functional gate conductors is a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance.
- [c19] The method of claim 12, wherein the length of said dummy gate conductors is a function of positive integer multiples of a

minimum length of said gate conductors and of positive integer multiples of said fixed distance.

- [c20] The method of claim 12, further including forming source/drains in said substrate underneath and proximate to said functional gate conductors.
- [c21] The method of claim 12, further including forming N-wells, P-wells or both N-wells and P-wells in said substrate underneath and proximate to said functional gate conductors.
- [c22] The method of claim 12, further including a forming a gate dielectric between said gate conductors and said substrate.
- [c23] A method of designing a device having a gate length and a gate width comprising:
providing a design grid of gate shapes, each gate shape having a fixed width defined by opposite ends and extending in a widthwise direction, a useable fixed width less than said fixed width and a fixed length extending in a lengthwise direction, said lengthwise direction substantially perpendicular to said widthwise direction, said gate shapes arranged substantially parallel to each other in said widthwise direction and periodically spaced apart a fixed distance in said lengthwise direction; and
forming a functional gate shape from one or more of said gate shapes.

- [c24] The method of claim 23, wherein gate shapes and portions of gate shapes not used to form said functional gate shape are left in place as dummy gate shapes not connected to said functional gate shape.
- [c25] The method of claim 23 further comprising, if said gate length is equal to said fixed length, connecting a whole number of gate shapes together along an end of each of said number of gate shapes, the number of gate shapes determined by dividing said gate width by said useable fixed width.
- [c26] The method of claim 23 further comprising, if said gate length is greater than said fixed length, determining a minimum positive integer and a new gate length such that said new gate length is greater than said gate length and said new gate length is equal to said minimum positive integer times the sum of said fixed length and said fixed distance.
- [c27] The method of claim 26, further including determining a new gate width by multiplying together the sum of said fixed length and said fixed distance, said minimum positive integer and said fixed gate width and dividing the result by said fixed gate length.
- [c28] The method of claim 27, further including connecting a number gate shapes equal to said minimum positive integer of gate shapes together along an end of each of said number of gate

shapes, each gate shape of said number of gates shapes having a width equal to said new gate width.

- [c29] The method of claim 23 further including, if said gate width divided by said useable gate length is less than 1, forming said functional gate from a gate shape of a length equal to said gate width.